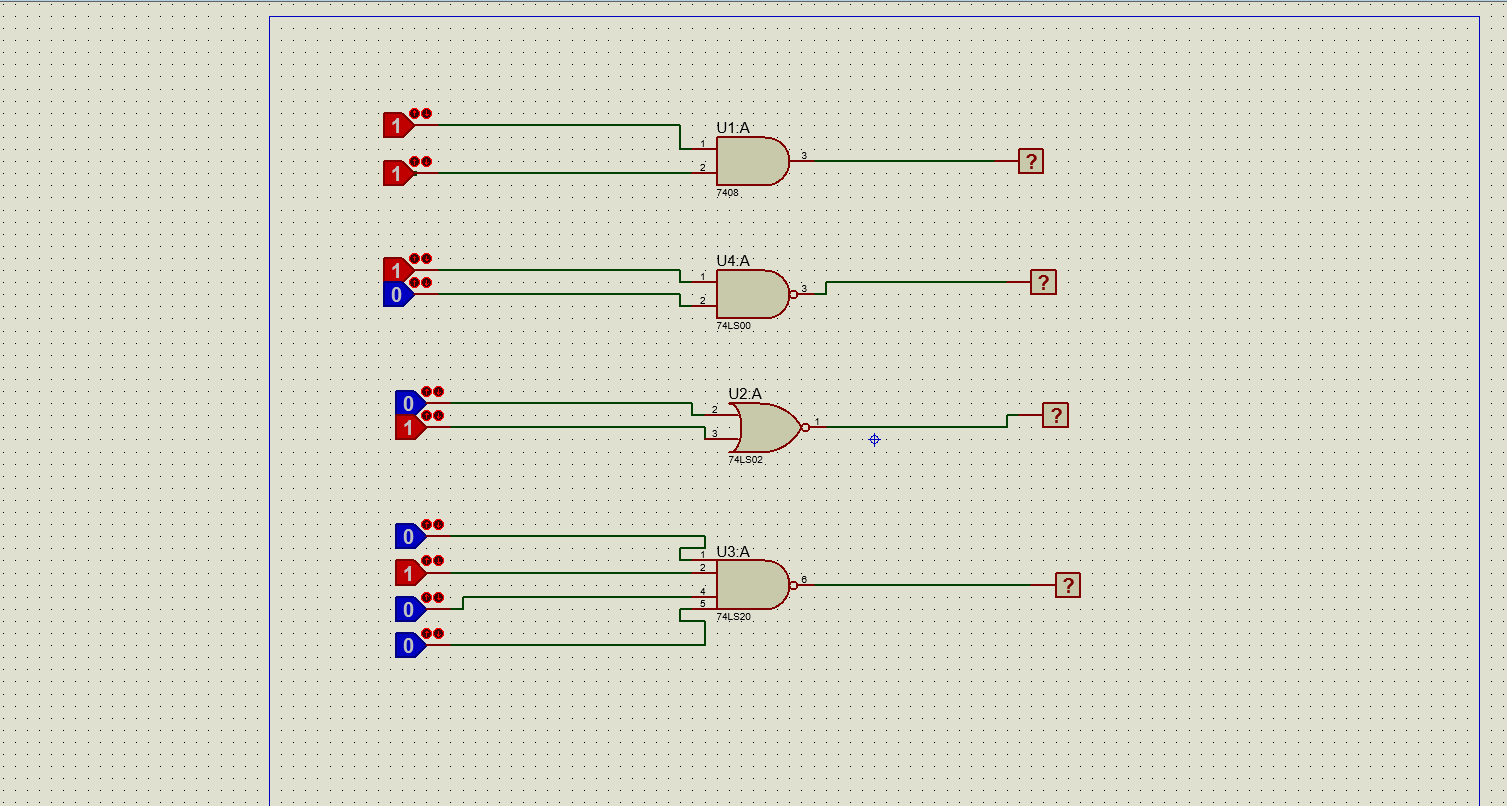
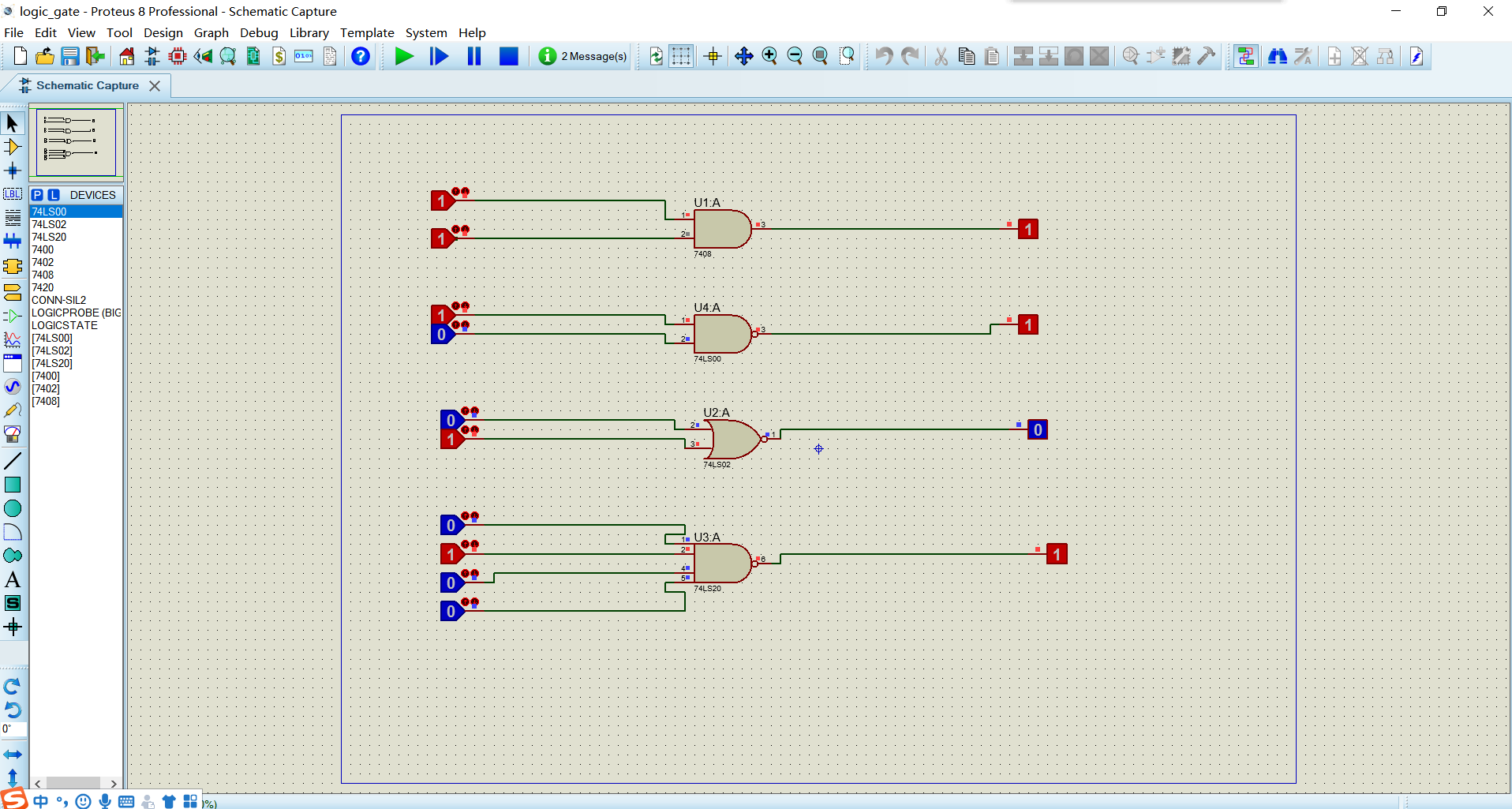
# 实验一 软件的使用

实验结论

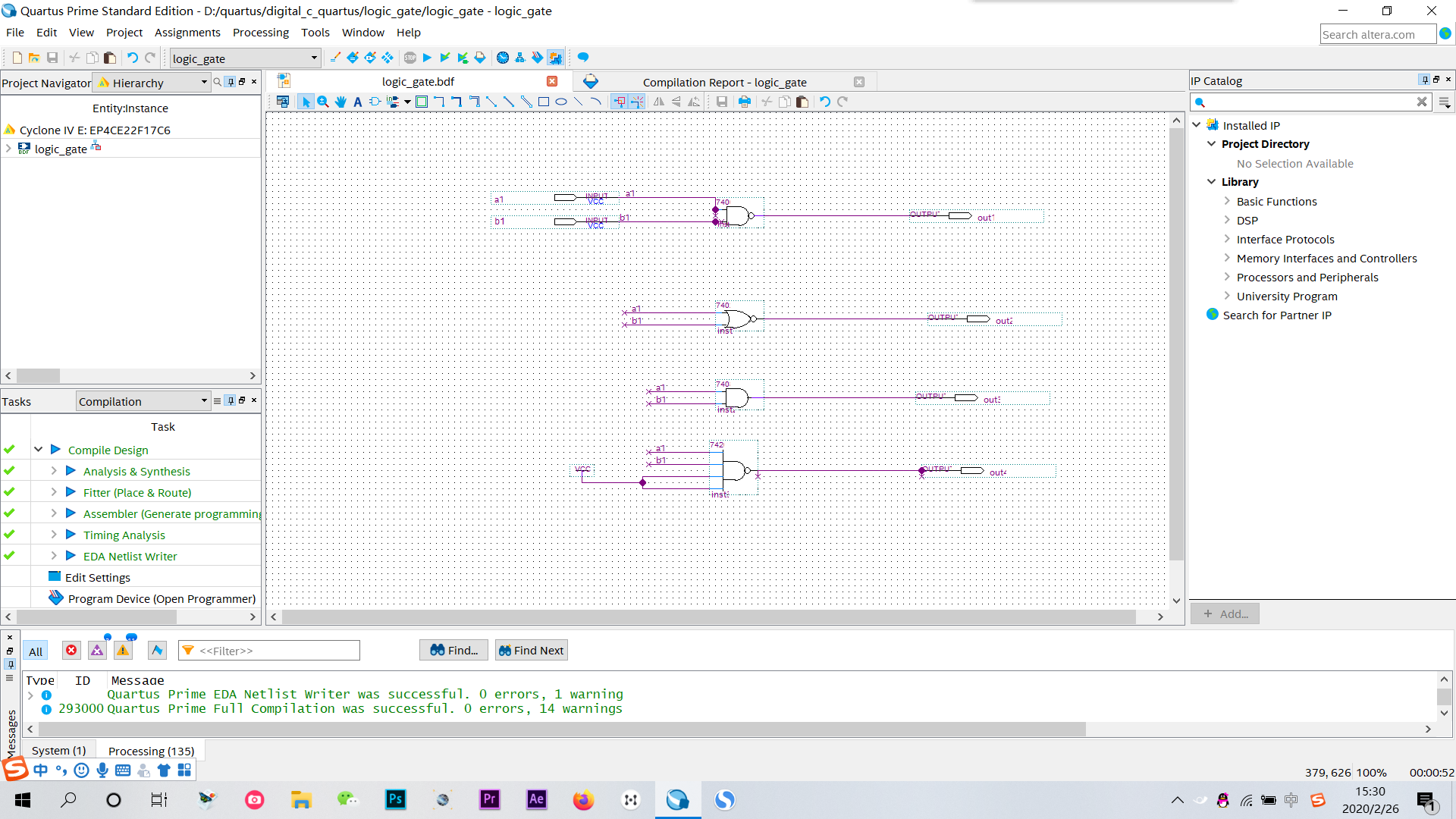
.1.Protues电路图



2.protues仿真效果图



1. Quartus顶层文件原理图



4.Quartus测试文件（完整测试代码）

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// \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

// This file contains a Verilog test bench template that is freely editable to

// suit user's needs .Comments are provided in each section to help the user

// fill out necessary details.

// \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

// Generated on "02/26/2020 19:55:58"

// Verilog Test Bench template for design : logic\_gate

//

// Simulation tool : ModelSim-Altera (Verilog)

//

`timescale 1 ns/ 1 ps

module logic\_gate\_vlg\_tst();

// constants

// general purpose registers

//reg eachvec;

// test vector input registers

reg a1;

reg b1;

// wires

wire out1;

wire out2;

wire out3;

wire out4;

// assign statements (if any)

logic\_gate i1 (

// port map - connection between master ports and signals/registers

.a1(a1),

.b1(b1),

.out1(out1),

.out2(out2),

.out3(out3),

.out4(out4)

);

initial

begin

// code that executes only once

// insert code here --> begin

a1=0;

b1=0;

#30

a1=1;

#50

b1=1;

#20

a1=0;

#10

b1=0;

// --> end

$display("Running testbench");

end

endmodule

5.quartus仿真效果图

